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32 BIT RIPPLE CARRY ADDERS USING CMOS DIFFERENTIAL LOGIC

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ABSTRACT
This paper describes a high speed boosted CMOS differential logic which is used in 32 bit ripple carry adders. The recommended logic style increases switching speed by boosting the gate–source voltage of transistors.Test sets of logic gates were designed in a 0.18-µm CMOS process, whose results indicated that the energy–delay product of the proposed logic style enhanced up to 50% compared with conventional logic styles with supply voltage of 1.8V. The simulation result indicates that 32 bit ripple carry adder designed by proposed logic style indicate that the addition time is less as compared to conventional CMOS circuits.

Keywords: Adder, Low Power, Low Voltage, Voltage Boosting, Addition Time

I. INTRODUCTION
Bootstrapping is an important method for speed improvement and reduction of power. One of the popular methods to reduce the power consumed by a CMOS digital circuit is supply voltage scaling. This is because of the switching power taking by the circuit has a quadratic relationship with supply voltage. In some cases, the circuit is made insuch a way to conduct in the sub threshold region for getting maximum energy efficiency.
Meanwhile this idea is limited and used in a low design end where speed is considered as the secondary concern because of severe speed degradation due to small switch current and variation of high performance since variations in process, temperature and threshold voltage. For implementing a medium and high end in which speed performance and efficiency of energy both acquired importance, no acceptance of enough aggressive voltage scaling and then a near threshold voltage design is more perfect for acquiring relatively large energy efficiency in the absence of severe speed degradation. The technique of voltage scaling helps in decreasing the total power consumed by a system. In certain applications where high speed is essential differential cascade voltage switch is avoided due to the insufficient speed of the circuit. However, domino logic is not accurate due to the decrease in overdrive voltage.As supply voltage scaling reaches the threshold voltage the performance of the speed of earlier CMOS circuits like static CMOS logic, differential cascade voltage switch (DCVS) logic[see Fig. 1(a)] and domino CMOS logic [see Fig. 1(b)] is degraded due to the decrease in overdrive voltage (VGS – VTH) of transistors. To reduce this problem, a bootstrapped CMOS containing large capacitive load driver was introduced. It was an alternative to problem of speed degradation. It can increase the switching speed at low supply voltage by giving the voltage of some inner nodes goes boosted beyond the supply rails. In this two capacitors are used for the purpose of bootstrapping. However this circuit was introduced touse as a driver of large capacitive load, logic functions cannot be sufficiently fit into the circuit and the merits of speed was not completely exploited. For fast logic operation with low supply voltage, BDL known as CMOS bootstrapped dynamic logic was introduced [see Fig.1(c)]. However, the speed of this BDL was not increased too much due to the fact of the latent bulky bootstrapped circuit which wassuperimposed over the entire circuit. Moreover, there is a limitation of construction of logic of this BDL since it is known as a one ended structure.

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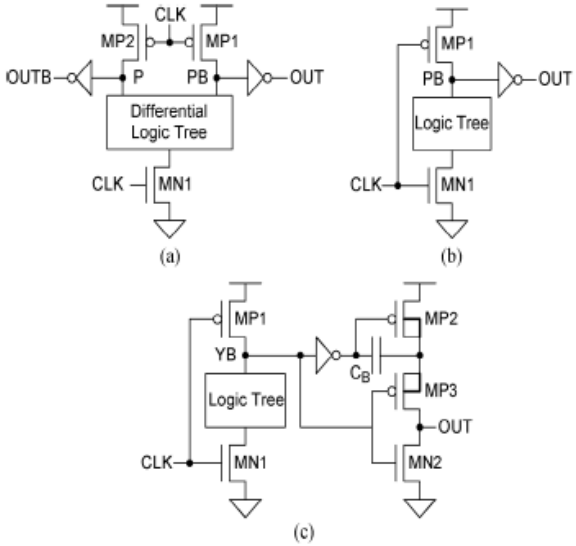
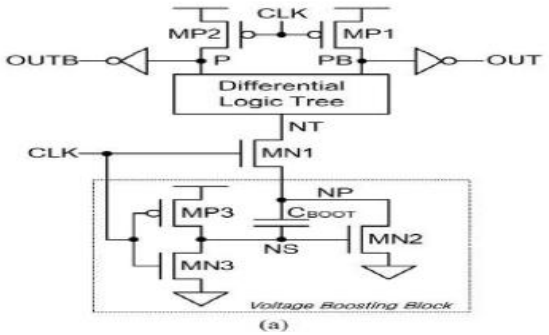


Fig. 1. Conventional digital CMOS circuits. (a) DCVS. (b) Domino CMOS logic. (c) BDL.

To eliminate the above problem BCDL differential logic style was introduced. It is not only good in terms of improving switching speed but also minimizes area due to sharing of single boosting circuit. Switching speed is improved due to the boosting of overdrive voltage along critical timing signal path. Meanwhile the problem of latency can be removed by allowing the block of voltage boosting directly to differential logic tree.



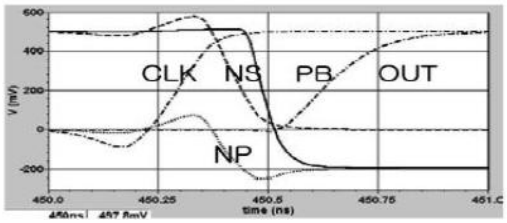


Fig. 2 (a) BCDL structure ***(b) Simulated waveforms***

It consist of a differential logic block known as precharged and a voltage boosting block. The circuit lower part is known as voltage-boosting block, which is given in the dotted box including transistors known as MN2, MN3, and MP3 and CBOOT known as boosting capacitor and is used in boosting of the voltage of NP reaches below the ground. The logic block which is known as precharged differential, is made of differential logic tree with bottom transistor named as MN1, precharge transistors known as MP1 and MP2 and output inverters gets the boosted voltage at NP and calculate the value of the output logic.Its operation is depend on two phases known as a precharge phase and boosted evaluation phase. The circuit is in precharge phase when the value of CLK goes to low. On precharge phase, there is a separation of the precharge differential logic block from the block of voltage boosting due to the turn of MN1. Precharge nodes P and PB that are in the differential logic block are precharged to the supply voltage with the help of MP1 and MP2 resulting in outputs named as OUT and OUTB low. On similar time, turn on of the transistors known as MP3 and MN2 in the voltage boosting block takes place that results in NS to high and NP to low. Then a voltage that is identical to the supply voltage is applied to CBOOT. When the value of CLK changes from low to high then the circuit appears into the boosted evaluation phase. The waveforms execution in this phase of BCDL are shown in Fig. in which supply voltage of 0.5V is used. When CLK value goes to high then there is a turn on of MN1 takes place and connection of the differential logic tree to the block of voltage boosting block is taking place. During this time there is a pull down toward the ground that result in boosting of NP and NT below the ground with the assistant of capacitive coupling carried by CBOOT. As given in Fig. , NP temporary approaches at -250 mV and settles

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down near -200 mV by the boosting action. However, a small forward in the voltage of source body maintained in these transistors using boosting source voltages reaches below the ground leads to decrease in threshold voltage of all these transistors increase their driving strength. Meanwhile, the boosted voltage that appears at NT is then goes to P or PB is pulled down below the ground. Then, there is an increase in the gate source voltage of the driver PMOS transistor enhances its driving strength. Effects of all these driving strength that is carried out with the help of boosting are then combined together along the critical time signal path that is taken from input to output by nodes ofprecharging that results in switching speed improvement at a low voltage regionThus it helps in improving switching speed and considered as a gooddifferential logic style that is utilized in high speed applications.

II. SIMULATION COMPARISION

Ripple carry chain consists of 8 bit was used in the BCDL adder that is used to boost the operation of each stage of carry chain meanwhile a carry chain consistof 8 bit Manchester was introduced in the adder of DCVS and BDL used for propagation of carry of high speed. Fig.3 shows the previous structure of 8 bit ripple carry chain that is used in the BCDL adder.

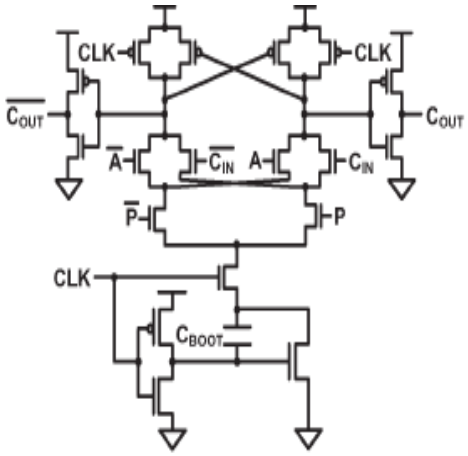

Fig.3. Conventional structure of 8 bit ripple carry chain used in BCDL

III. XOR GATE

Carry is propagated due to the help of XOR gate when the value of both the inputs are 1 whereas it is generated when the value of either of its input are 1.Fig.4 shows the structure of XOR gate that is used for carry propagation.

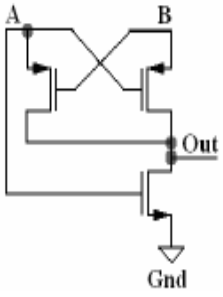

Fig. 4. XOR gate

$P_i = A_i$ xor B_i (1)

Table 1 shows the total delay, power consumption and power delay product of proposed 1 bit ripple carry adder as compared with conventional 1 bit ripple carry adder.

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Table 1- 1 bit ripple carry adder

Ripple Carry Adder	Rising delay (*)	Falling Delay (*)	Total delay(*)	Power consumption(*)	PDP (&)
22T (Prop.)	-39	.088	19.54	16	313
24T	-39	.22	19.61	16	314
Units- *=ns, &=ns x ns					

Fig.5 shows the rising delay, propagation delay, power consumption and power delay products chart of 1 bit ripple carry adder.

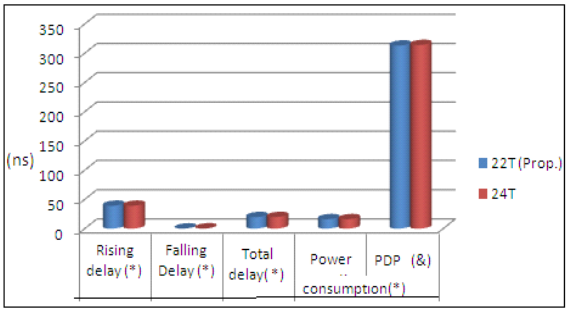

Fig. 5. Rising delay, propagation delay, power consumption and PDP chart of 1 bit ripple carry adder.

IV. EXPERIMENT RESULTS

The experimental result is for 32 bit ripple carry adder using the proposed logic style. In 32 bit adder an 8 bit ripple carry chain is used for boosting operation at each carry chain stage. Fig. 6 shows the proposed 8 bit ripple carry chain in BCDL.

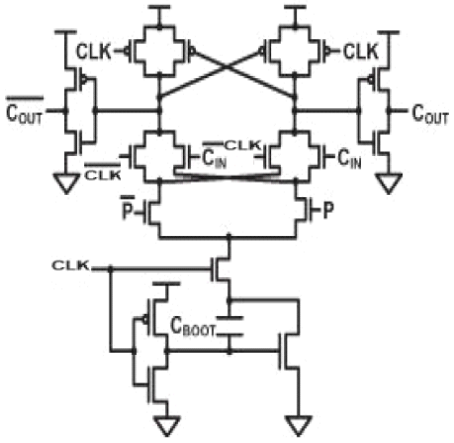

Fig.6. Proposed 8 bit ripple carry chain in BCDL

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The proposed structure of 1 bit ripple carry chain in 32 bit BCDL adder is shown in Fig.7

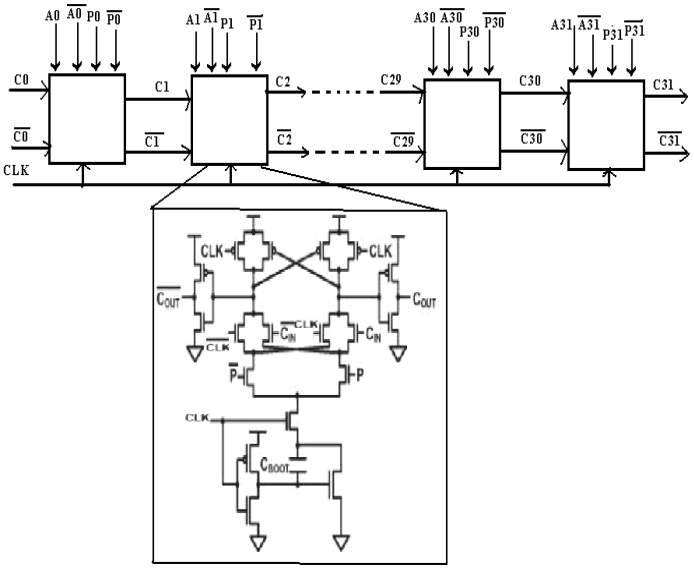

Fig. 7. Structure of 1 bit ripple carry chain in 32 bit BCDL adder

Table 2 shows the total delay, power consumption and power delay product of 32 bit ripple carry adder.

Table. 2. 32 bit ripple carry adder

32 bit Ripple Carry Adder	Rising delay (*)	Falling Delay (*)	Total delay(*)	Power consumption($)	PDP (&)
704T (Prop.)	.39	.14	19.57	10	195
768T	.39	.22	19.61	10	196
Units- *=ns, &=ns x ns $=µm					

The rising delay, propagation delay, power consumption and PDP chart of 32 bit ripple carry adder is shown in Fig.8

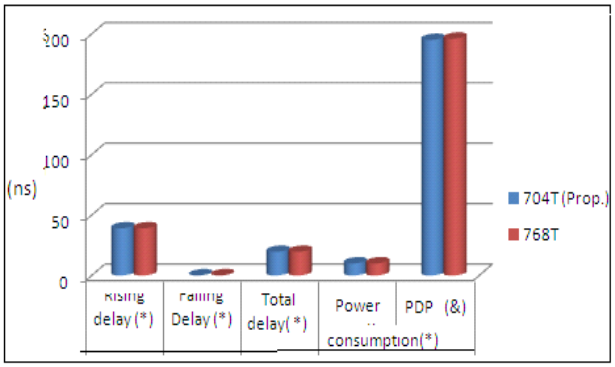

Fig.8 Rising delay, propagation delay, power consumption and PDP chart of 32 bit ripple carry adder

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The proposed 8 bit ripple carry adder waveform shown in Fig. 9

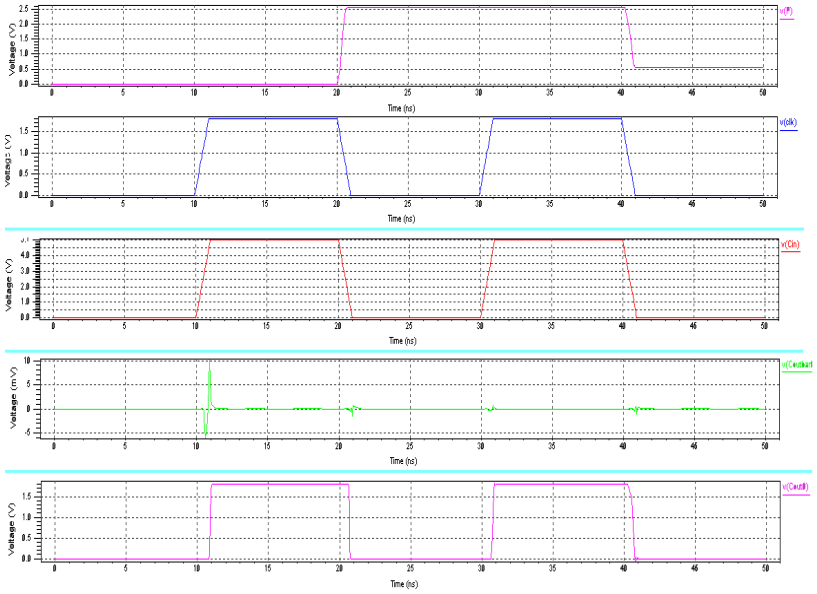

Fig. 9 Proposed 8 bit ripple carry adder waveform

V. CONCLUSION

CMOS differential logic style having feature of voltage boosting has been described. The BCDL provides increase in switching speed when it is compared to conventional logic style at low supply voltage with the help of a single boosting circuit that isshared by complementary outputs. The BCDL also minimizes the area. Comparison results is carried out in tsmc 0.180 um cmos process whichshows that the energy delay product of the suggested logic style was better when compared with the previous logic styles. The experiment result for a 32 bit ripple carry adder consist of BCDL logic style shows a decrease in the addition time.

VI. REFERENCES

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